DZero Run IIb Risk Analysis

A qualitative process of risk assessment was used, based on a method described in "A Guide to the Project Management Body of Knowledge"[1]. For each WBS Level 4 element, the potential impacts of the element's risk to the cost, schedule, scope, and technical concerns of the project were assessed by Level 2 project managers and assigned a numeric value according to the severity of the potential impact. Table 1 summarizes the criteria used for this "severity of impact" assessment. The numeric values and the definitions assumed for each level of impact are shown.

Once the severity of impact was determined, then a probability of that impact occurring was assigned and a "risk score" was determined for each "project objective" (cost, schedule, scope, and technical). This risk score was the product of the impact severity and the probability. The resulting risk score was used to categorize the risk as low, medium or high for each WBS Level 4 element and project objective. Table 2 shows this probability-impact matrix and the risk score "cuts" used to define low, medium, or high risk.

For any "high-risk" elements, possible risk mitigation measures were considered and described under the "risk mitigation" heading of the WBS Dictionary entry for that WBS element. The following pages taken from the project schedule show the results at WBS level 4 for these risk assessments, with color-coded indicators denoting the level of risk that was determined.

Table 1 – Risk Impact Table

Project Objective	Very Low Impact .05	Low Impact .1	Moderate Impact .2	High Impact .4	Very High Impact .8	Comments
Cost	Insignificant cost increase	<5% cost increase	5-10% cost increase	10-20% cost increase	>20% cost increase	
Schedule	Insignificant schedule slippage	Schedule slippage <5%	Overall project slippage 5-10%	Overall project slippage 10-20%	Overall project schedule slips>20%	20% slippage ~ 8 months
Scope	Scope decrease barely noticeable	Minor areas of scope affected	Major areas of scope affected	Project scope reduction unacceptable for physics objectives	Scope of project effectively useless for physics objectives	
Technical	Technical degradation of project barely noticeable	Technical performance of final product minimally affected	Technical performance of final product moderately affected	Degradation of technical performance of final product unacceptable for physics objectives	Technical performance of project end item effectively useless for physics objectives	

Table 2- Probability-Impact Matrix (green=low, yellow=medium, red=high)

Probability	Risk Score = Probability x Impact				
0.9	0.05	0.09	0.18	0.36	0.72
0.7	0.04	0.07	0.14	0.28	0.56
0.5	0.03	0.05	0.10	0.20	0.40
0.3	0.02	0.03	0.06	0.12	0.24
0.1	0.01	0.01	0.02	0.04	0.08
	0.05	0.10	0.20	0.40	0.80
	Impact on Objectives				

[1] A Guide to the Project Management Body of Knowledge, 2000 Edition, Project Management Institute, Four Campus Boulevard, Newton Square, PA.

AFE/Trip Upgrade – Risk Analysis

The AFE II/TriP upgrades to the Central Fiber Tracker (CFT) front end contain limited risk. The boards themselves are upgrades to, and simplifications of, the Run IIa versions, which are installed and operating in the current detector. The system as a whole will provide more uniform and stable noise performance, which will aid in tracking and triggering efficiency. The next generation of the TriP chip will also provide information on the z-coordinate of the tracks, offering additional segmentation for track reconstruction and triggering purposes. Both issues are of particular concern after the cancellation of the Run IIb silicon, which will result in increased challenges for tracking in a high luminosity environment. We have had extensive experience with readout from the CFT, and our M&S, labor, and technical assessments of what will be required to complete the project are based very closely on this experience.

Based as it is on our previous experience, we consider the technical challenges associated with the boards themselves and the new trigger chip to relatively low. Indeed, the first prototype of the TriP chip worked as expected after the first submission, a notable success for an integrated circuit of this complexity. An additional submission is needed primarily to integrate the capability for providing timing information, which will allow us to determine the z-coordinate of tracks. Prototypes for the new version of the Analog Front-End boards (AFE II) are being laid out now, and few technical problems are anticipated.

The M&S costs for both the AFE II and the TriP are well understood. The TriP has been successfully submitted before, and the cost for the boards and associated parts is based directly on the Run IIa version, which is very well understood. We consider the primary cost risk for the AFE II/TriP upgrade to be that associated with the labor. Any unforeseen difficulties in the prototyping, or unanticipated rework of the production boards (a not uncommon post-production necessity) will require labor by definition not accounted for in the base estimate. We have taken this uncertainty into consideration in the assignment of the 70% contingency in the labor for this sub-project, which is discussed in the cost and contingency document that has been provided.

AFE/TRIP Upgrade Risk Scores (Probability x Impact)			
Cost	**Schedule**	**Scope**	**Technical**
0.3 x 0.2 = 0.06	0.3 x 0.1 = 0.03	0.1 x 0.1 = 0.01	0.1 x 0.1 = 0.01

Layer 0 Silicon Risk Analysis Summary

ID	WBS	Name	Cost Risk Score	Schedule Risk Score	Scope Risk Score	Technical Risk Score
1	**1.6**	**Layer 0 Silicon Detector**				
2	**1.6.1**	**Sensors**	🟡	🟡	🟢	🔴
16	**1.6.2**	**Readout Electronics**				
19	**1.6.2.3**	**Hybrids**	🟢	🟢	🟢	🟡
40	**1.6.2.4**	**Analog Cables**	🟡	🟢	🟢	🟡
49	**1.6.2.5**	**Flex Grounding Circuits**	🟢	🟢	🟢	🟢
54	**1.6.2.6**	**Digital Cables**	🟢	🟢	🟢	🟢
64	**1.6.2.7**	**Twisted-Pair Cables**	🟢	🟢	🟢	🟡
74	**1.6.2.8**	**Junction Cards**	🟢	🟢	🟢	🟢
82	**1.6.2.9**	**Adapter Cards**	🟡	🟢	🟡	🟡
95	**1.6.2.10**	**High-Voltage System**	🟢	🟢	🟢	🟢
100	1.6.2.11	Readout Chain Integration	🟢	🟢	🟢	🟢
101	**1.6.2.12**	**Full Chain Tests**	🟢	🟢	🟢	🟡
108	**1.6.3**	**Mechanical Design and Fabrication**				
109	**1.6.3.1**	**Support Structures Design**	🟢	🟢	🟢	🟡
117	1.6.3.2	Development and integration of design (FNAL)	🟢	🟢	🟡	🟡
122	**1.6.3.4**	**Final Fabrication Tooling**	🟢	🟢	🟢	🟢
126	**1.6.3.5**	**Final Quality Assurance Tooling**	🟢	🟢	🟢	🟢
131	**1.6.3.7**	**Final Support Structures Production**	🟢	🟢	🟢	🟡
140	**1.6.4**	**Layer 0 Detector Modules**				
143	**1.6.4.3**	**Production Module Fixtures**	🟢	🟢	🟢	🟢
150	**1.6.4.4**	**Preproduction Modules**	🟢	🟡	🟢	🔴
155	**1.6.4.6**	**Module Production**	🟢	🔴	🟢	🔴
169	**1.6.5**	**Final Detector Integration and Assembly**				
170	**1.6.5.1**	**Layer 0 Support Structure Holding Fixtures**	🟢	🟢	🟢	🟢
174	**1.6.5.2**	**Layer 0 Module Installation Fixtures**	🟢	🟢	🟢	🟢
180	1.6.5.5	Mount layer 0 sensor modules	🟢	🟡	🟢	🟡
192	**1.6.5.17**	**Monitoring**	🟢	🟢	🟢	🟢
194	1.6.5.18	Software and Simulation	🟢	🟢	🟢	🟢

Trigger Run IIb Risk Analysis Summary

ID	WBS	Name	Cost Risk Score	Schedule Risk Score	Scope Risk Score	Technical Risk Score
1	1.2	Run IIb Trigger Upgrade				
2	1.2.1	Level 1 Calorimeter Trigger				
3	1.2.1.1	ADC/Digital Filter (ADF)	Red	Yellow	Green	Green
29	1.2.1.2	ADF Crates	Yellow	Green	Green	Green
40	1.2.1.3	Trigger Algorithm Board	Red	Yellow	Green	Green
60	1.2.1.4	Global Algorithm Board (GAB)	Yellow	Yellow	Green	Green
80	1.2.1.5	Cables	Yellow	Green	Yellow	Yellow
84	1.2.1.6	TAB Crates and Services	Green	Green	Green	Green
94	1.2.1.9	Prototype Integration	Green	Red	Green	Green
102	1.2.1.10	Pre-Production Integration	Green	Red	Green	Green
109	1.2.1.11	L1 Cal Online Software	Green	Yellow	Yellow	Yellow
113	1.2.2	Level 1 Calorimeter Track Matching				
120	1.2.2.4	SLDB	Green	Green	Green	Green
124	1.2.2.5	MTCxx	Green	Green	Green	Green
134	1.2.2.6	MTCM	Green	Green	Green	Green
140	1.2.2.7	MT Flavor Board	Green	Green	Green	Green
153	1.2.2.8	Infrastructure	Green	Green	Green	Green
169	1.2.3	Level 1 Tracking				
171	1.2.3.2	Develop Target CTT Algorithm	Yellow	Yellow	Yellow	Yellow
175	1.2.3.4	Develop Test Procedures	Green	Green	Green	Green
178	1.2.3.5	DFEA Preproduction I	Yellow	Yellow	Red	Yellow
190	1.2.3.6	DFEA Preproduction II	Yellow	Yellow	Red	Yellow
206	1.2.3.7	DFEA Production	Red	Yellow	Green	Red
229	1.2.4	Level 2 Beta Processor				
230	1.2.4.1	Finalize Targets For Run2b Beta Upgrades	Green	Yellow	Green	Green
240	1.2.4.2	Develop Prototype	Yellow	Green	Green	Green
255	1.2.4.3	Test Prototype	Green	Green	Green	Green
263	1.2.4.4	Assemble Production Processors	Yellow	Green	Green	Green
270	1.2.5	Silicon Track Trigger Upgrade				
275	1.2.5.4	VME Motherboard	Green	Green	Green	Green
283	1.2.5.5	STC Module	Yellow	Yellow	Green	Green
291	1.2.5.6	VTM	Red	Green	Green	Green
296	1.2.5.7	Link Transmitter Board	Green	Green	Green	Green
304	1.2.5.8	Link Receiver Board	Green	Green	Green	Green
312	1.2.5.9	BC Module	Green	Green	Green	Green
320	1.2.5.10	TFC Module	Yellow	Yellow	Green	Green
327	1.2.5.11	Hotlink Repeaters	Green	Green	Green	Green
332	1.2.5.12	LVDS Cables	Green	Green	Green	Green
336	1.2.5.13	Splitters	Green	Green	Yellow	Yellow
341	1.2.5.14	Fibers	Green	Green	Yellow	Yellow
347	1.2.5.16	STC firmware	Red	Green	Green	Green
349	1.2.5.17	TFC Code	Green	Green	Green	Green
351	1.2.5.18	Downloading & Monitoring	Green	Green	Green	Green
355	1.2.6	Trigger Simulation				
364	1.2.6.3	L1CTT Simulation	Green	Yellow	Yellow	Green
372	1.2.6.4	STT Simulator	Green	Green	Green	Green

ID	WBS	Name	Cost Risk Score	Schedule Risk Score	Scope Risk Score	Technical Risk Score
1	1.3	Online Systems				
2	1.3.1	Level 3 Systems	🔴	🟢	🟢	🟢
56	1.3.2	Network and Host Systems				
57	1.3.2.1	Online/DAQ Network	🟢	🟢	🟢	🟢
62	1.3.2.2	Control Room Nodes	🟢	🟢	🟢	🟢
75	1.3.2.3	Monitoring Nodes	🟢	🟢	🟢	🟢
88	1.3.2.4	Storage Systems	🟢	🟢	🟢	🟢
114	1.3.2.5	HOST Systems R&D	🟢	🟢	🟢	🟢
120	1.3.2.6	DAQ HOST Systems	🟢	🟢	🟢	🟢
131	1.3.2.7	ORACLE Systems	🟢	🟢	🟢	🟢
143	1.3.2.8	File Servers	🟢	🟢	🟢	🟢
156	1.3.2.9	OS & Software	🟢	🟢	🟢	🟢
161	1.3.3	Control Systems	🟡	🟢	🟢	🟢
178	1.3.4	DAQ/Online Management	🟢	🟢	🟢	🟢

Risk Mitigation

LAYER 0 SILICON DETECTOR

This section discusses possible ways to mitigate the risks for those deliverables in the Layer 0 silicon project plan that received high ($\geq$ 0.18) risk scores.

WBS 1.6.1 Sensors

The technical risk was classified as "high" for the silicon sensors. The major concern is that the preferred vendor (Hammamatsu) will decline to produce the relatively small quantity of sensors needed (96). Hammamatsu had begun delivering production batches of L2-L5 sensors on schedule for the recently cancelled Run 2b replacement detector and also had delivered high-quality sensor prototypes that met the specifications for the L1 layer of that detector. The new Layer 0 detectors will be technically very similar to those designed and prototyped for L0/L1, differing mainly in geometrical parameters such as sensor strip pitch, length, and width. Should Hammamatsu decline this small production order, or agree to produce it but at an unacceptable cost, an alternate vendor would have to be found and qualified. Alternate vendors are available, but sensor quality has been found to vary considerably among vendors. In addition, a switch to another vendor is likely to result in some moderate schedule delay, given that procurement actions that have already taken place with Hammamatsu would have to take place with a different vendor. Thus, while not the preferred solution, alternate sensor vendors serve as the principal means by which the technical risk is mitigated.

WBS 1.6.4.4 Preproduction Modules (Layer 0)

The technical risk was classified as "high" for the pre-production modules. This task involves the assembly of sensors, analog flex cables, and hybrids into pre-production units that can be mounted onto a carbon fiber support structure. Technical concerns include wirebonding and the making of other electrical connections, grounding issues, and the follow-on assembly and mounting under tight spatial constraints. The technical risk has been partially mitigated by the prototyping work already done for the L0/L1 run 2b detector. Further mitigation of the risk will occur through the grounding studies that will be done as part of the Run IIb closeout, and the making of a sufficient number of mechanical and electrical grade pre-production modules to develop and validate procedures and tooling.

WBS 1.6.4.6 Module Production (Layer 0)

The technical risk and schedule risk were classified as "high" for the production modules. This task involves the assembly of sensors, analog flex cables, and hybrids into the final production units that can be mounted onto the carbon fiber support structure. Technical concerns include wirebonding and the making of other electrical connections, grounding issues, and the follow-on assembly and mounting under tight spatial constraints. The technical risk will be mitigated by the pre-production module work. The schedule risk can be mitigated by the possibility of additional shifts and /or assembly stations during the assembly process.

TRIGGER

The original trigger baseline risk mitigation information, shown below, has been updated with some additional comments based on the current status, for those deliverables that received high risk scores in the baseline trigger schedule.

WBS 1.2.1.1 ADC/Digital Filter (ADF)

Risk Mitigation

Risk of escalation in parts cost due to unforeseen design changes is mitigated by the relatively large contingency assigned to the procurement of components and fabrication/assembly given the advanced state of the design (prototype design nearly finished). Cost risk from extra labor needed to complete the project is reduced because of the large fraction of the labor that is covered by in-kind contributions from Saclay. Extra Saclay personnel can be diverted to the project should the need arise.

Comment – The cost risk was classified as "high" for the ADF. Following the cancellation of the Run 2b silicon detector project the Saclay group has decided not to pursue the ADF project beyond the prototyping phase. The remaining cost for the production phase will be funded by DOE equipment funds, rather than in-kind contributions, and the work will be performed at U.S. universities.

WBS 1.2.1.3 Trigger Algorithm Board

Risk Mitigation

Risk of escalation in parts cost due to unforeseen design changes is mitigated by the relatively large contingency assigned to the procurement of components and fabrication/assembly given the advanced state of the design (prototype layout started). Cost risk from extra labor needed to complete the project is reduced because of the large fraction of the labor that is covered by in-kind contributions from Columbia/Nevis. Extra Nevis personnel can be diverted to the project should the need arise.

Comment- The cost risk was classified as "high" for the TAB. A prototype TAB has been completed and successfully tested. Procurements for a pre-production TAB are expected to begin in early CY04. Therefore, the cost risk has been reduced.

WBS 1.2.1.9 Prototype Integration

Risk Mitigation

The impact of integration taking longer than expected is reduced by putting this task as early in the project as possible. Additionally, prototype integration tests are planned to mimic as closely as possible data taking in the D0 environment, including the use of real data from the BLS (via splitter cards) and real timing signals from the Trigger Framework.

Comment- The schedule risk was classified as "high" for the prototype integration. The first phase of integration testing (ADF/TAB) has been completed successfully, so the schedule risk is reduced.

WBS 1.2.1.10 Pre-Production Integration

Risk Mitigation

Impact on the schedule of mis-estimates of the time required to complete this task is minimized by performing as much of the integration as possible with prototype boards (1.2.1.9).

Comment- The schedule risk was classified as "high" for the pre-production integration. This set of tasks has not yet begun, and the risks remain unchanged.

WBS 1.2.3.5 DFEA Preproduction I

Risk Mitigation- n/a

Comment- The scope risk was classified as "high" for the DFEA I preproduction. This phase is almost complete.

WBS 1.2.3.6 DFEA Preproduction II

Risk Mitigation- n/a

Comment- The scope risk was classified as "high" for the DFEA II preproduction. This phase remains to be done and the risk remains unchanged.

WBS 1.2.3.7 DFEA Production

Risk Mitigation

Cost: There are 3 factors which may affect the "Cost":

1) Xilinx chip prices may not completely follow vendor projected quote.
2) We may need XC2V8000 chips due to equation growth when we put in effects of various inefficiencies and misalignments in the modeling of the CFT in the simulations.
3) The board will use parts which are a factor of 2.5 denser and complicated than the current Run2a DFEA boards. This may lead to higher vendor quotes for PCB fabrication and assembly compared to Run2a quotes included in the BOE.

All of these factors may lead to a cost increase which is a significant fraction of project cost. We have addressed these risks by including a 70% contingency on the XC2V FPGA costs, a 30%contingency on the PCB fabrication, and a 50% contingency on the production parts.

Comment- The cost and technical risk were classified as "high" for the DFEA production. Cost risk is now slightly reduced due to a better sense of the vendor costs for PCB fabrication from the pre-production work.

WBS 1.2.5.6 VTM

Risk Mitigation:

The VME transition module has four Finisar optical receivers and HP g-link serial-to-parallel converters. Some parts used on this board (among them the Finisar receivers) are about to become obsolete. This board was difficult to design and the redesign required if different parts have to be used could mean significant engineering costs. To minimize this risk we intend to purchase the six boards required for the Run 2B upgrade plus 4 spares as soon as possible.

Comment- The cost risk was classified as "high" for the VTMs. These items have been procured, tested, and are ready for use. No remaining risk is associated with this item.

WBS 1.2.5.16 STC firmware

Risk Mitigation:

The scope of this item is not yet that well defined, since the systems that provide inputs to the STT are all being redesigned for the upgrade. The engineering budgeted in this item will also serve as contingency in case any layouts have to be revised to accommodate changes due to obsolete parts. To mitigate this risk, I have assigned 100% contingency for this task.

Comment- The cost risk was classified as "high" for the STC firmware. The risks remain unchanged for this item.